REMARKS

This amendment is being filed along with a Request for Continued Examination (RCE) application in response to the final Office Action having a mailing date of April 5, 2006. The independent claims are amended as shown. Claims 10 and 13-14 were previously canceled. No new matter has been added by this amendment. With this amendment, claims 1-9, 11-12, and 15-23 are pending in the application.

I. Preliminary Comments

In the final Office Action, claims 1-3, 5, and 8-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Partovi et al. (U.S. Patent No. 5,963,059). Claims 1-9, 11-12, and 15-23 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Nilsson (U.S. Patent No. 6,605,935) in view of Pricer (U.S. Patent No. 5,673,005).

Specifically in the final Office Action, the Examiner found the applicants' prior arguments to be unpersuasive. That is, the applicants previously argued, *inter alia*, that none of the cited references disclosed, taught, or suggested a symmetrization element having two transistors coupled in series or two transistors in a same circuit branch. The Examiner rejected the applicants' arguments for the reasons set forth in the final Office Action.

The applicants have now further considered the Examiner's position and believe that the claims in their current form do indeed distinguish over the cited references. However, to facilitate prosecution, the previous amendments and arguments are being replaced herewith by new amendments and arguments that are believed to more accurately reflect the distinctions between the cited prior art and the claimed subject matter.

In view of the amendments above and the arguments below, it is respectfully submitted that the claims are now further allowable over the cited references. Therefore, the applicants respectfully request that the rejections be withdrawn and the pending claims be allowed.

II. Discussion of the Applicants' Disclosed Embodiments and the Cited References

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

One embodiment disclosed by the present applicants is shown in Figure 5 of the present application. In Figure 5, a symmetrization element 230 is coupled to the output terminals (such as the outputs UP and DW) of the first and second bistable elements (such as the flip-flops 200a and 200b), with the symmetrization element 230 including two transistors N3 and N4 having control terminals coupled to the respective output terminals of the first and second bistable elements.

In a particular example, one transistor (*e.g.*, the transistor N4) has its gate terminal coupled to the output UP of the flip-flop 200a, and the other transistor (*e.g.*, the transistor N3) has its gate terminal coupled to the output DW of the flip-flop 200b. Thus, the symmetrization element 230 includes "first and second transistors, the first transistor having a control terminal coupled to the output terminal of the first bistable element and having a first terminal, the second the transistor having a control terminal coupled to the output terminal of the second bistable element and having a first terminal coupled to the first terminal of the first transistor." *See, e.g.*, Figure 5 of the present application.

In pages 2-3 of the present Office Action, the Examiner states that Partovi discloses the "symmetrization element" corresponding to the two inverters 830 and 832 (in his Figure 8). According to the Examiner, Figure 8 of Partovi represents "two transistors coupled in series (*i.e.*, same branch) having gates coupled to a common node" (emphasis ours). More specifically, the Examiner has interpreted each inverter of Partovi as including two transistors having gates coupled to a common node, and Partovi has no further detailed elaboration as to how the terminals of such transistors are coupled.

With regards to the other cited references, the Examiner has cited the transistors 34 and 35 in Figure 3 of Pricer. However, the present applicants respectfully note that the transistors 34 and 35 of Pricer clearly have their control terminals coupled to a common node 42.

As recognized by the Examiner on page 4 of the final Office Action, Nilsson does not disclose, teach, or suggest specific transistors in a symmetrization element.

III. Discussion of the Claims

Independent claim 1 has been amended to recite, *inter alia*, that the symmetrization element includes "first and second transistors, the first transistor having a control terminal coupled to the output terminal of the first bistable element and having a first terminal, the second the transistor having a control terminal coupled to the output terminal of the second bistable element and having a first terminal coupled to the first terminal of the first transistor." As explained above, this feature is not disclosed, taught, or suggested by any of the cited references, whether singly or in combination.

For example, Partovi does not show first and second transistors in either (or both) of his inverters 830 or 832 that have the features recited in claim 1. Even assuming hypothetically (as the Examiner has done) that Partovi's inverter 830 does include first and second transistors, then there is nothing further (beyond a standard inverter configuration) that can be gleaned from Partovi as to how the various terminals of such transistors may be specifically coupled.

Indeed, the Examiner has assumed that such transistors of Partovi would have "gates coupled to a common node." *See, e.g.*, page 3, line 3 of the final Office Action. That is, since the elements 830 and 832 in Partovi are described as "inverters," then such inverters would be expected to have a standard configuration (such as the inverter 23 of Pricer, which is comprised of the transistors 34 and 35 in his Figure 3 having control terminals coupled to a common node 42). The "common node" in Partovi would be the input terminal of his inverter 832, and that input terminal is in turn coupled to both of the gates of the two transistors in that inverter 832. As seen clearly, in Figure 8 of Partovi, that input terminal of his inverter 832 may perhaps be construed as being coupled to the element 804 (and hence both gates of the two transistors in the inverter 832 are coupled to the element 804)—BUT that input terminal of Partovi's inverter 832 can in no way be construed as being coupled to the element 802. This same scenario holds true with regards to Partovi's inverter 830 (*i.e.*, the two transistors in the

inverter 830 have gates coupled to a common node, which is coupled to the element 802 but not to the element 804).

Therefore, the gates of Partovi's two transistors (in his inverter 830 or 832) are coupled to a common node, and not with one gate in an inverter coupled to the element 804 and another gate of that same inverter coupled the element 802. In comparison, claim 1 as amended recites that the control terminal of the first transistor is coupled to the output terminal of the first bistable element and that the control terminal of the second transistor is coupled to the output terminal of the second bistable element. As depicted by way of illustrative and non-limiting example in Figure 5 of the present application, the control terminals of the transistors N3 and N4 are respectively coupled to the terminals DW and UP, which are not at a common node. Accordingly, claim 1 is allowable over Partovi.

Claim 1 as amended further recites coupling of the first terminals of the first and second transistors. This recitation, along with the recitations pertaining to the control terminals discussed above, is simply not disclosed, taught, or suggested by Partovi in a manner sufficient to anticipate claim 1. Furthermore, this recitations distinguishes over a possible reading of Partovi in which the first transistor is construed as being from the inverter 830 and the second transistor is construed as being from the inverter 832—this recitation in claim 1 requires the first and second terminals to be coupled to each other via their first terminals—this configuration is not possible in Partovi if one tries to construe the first transistor as belonging to the inverter 830 and the second transistor as belonging to the second inverter 832, since the logic gate 828 prevents such coupling of the two transistors of two different inverters. Accordingly, claim 1 is further allowable over Partovi.

With regards to Nilsson and Pricer, Nilsson does not have first and second transistors as recited in claim 1. Pricer does not cure the deficiencies of Nilsson. For example, and as explained above, the transistors 34 and 35 of Pricer have control terminals coupled to a common node. In contrast, claim 1 as amended recites that the control terminals of the first and second transistors are coupled (respectively) to output terminals of the first and second bistable elements. Accordingly, claim 1 is allowable over Nilsson and Pricer, whether singly or in combination.

Independent claims 5, 8, and 15-16 are amended in a manner generally similar to claim 1 above. For similar reasons explained above, such independent claims are allowable over Partovi, Nilsson, and Pricer, whether singly or in combination.

Independent method claim 9 has been amended to recite "using the symmetrization element having said first and second transistors that have their first terminals coupled to each other and that have their control terminals respectively coupled to the output terminals of the first and second bistable elements." Since these features are not disclosed, taught, or suggested by the cited references, claim 9 is allowable.

## IV. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

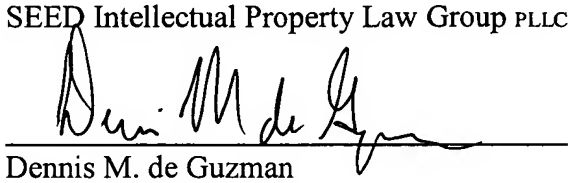
If the applicants' attorney Dennis M. de Guzman has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the Mr. de Guzman at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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